structure. The layout of the self-aligned contact structure can be square, rectangular, or long-for local interconnection, and can form a butted contact. It is understood by those skilled in the art that the conductive plug **322** can be adjacent to a gate structure, adjacent to the edge of an active region, or can cross the border between an active region and a field oxide region.

[**0022**] A metal layer is deposited and pattern-etched to form a metal interconnect **324** above the inter-level dielectric layer **320**. Electrical connection is made from the metal interconnect **324**, through the conductive plug **322**, to the salicide source/drain contact **318**.

[**0023**] The present invention avoids the dilemma of choosing between a salicide layer on the poly-silicon gate conductor and a self-aligned contact on the source/drain regions in the conventional art. In this embodiment, since the gate conductor **308** is made of metal, no salicide layer is needed for improving its interface quality with a metal interconnection structure. This naturally solves the dilemma by choosing to from the self-aligned contact **318** atop the source/drain regions **316**, without sacrificing the contact quality of the metal gate conductor **308**. In addition, by keeping the cap layer **312** atop the metal gate conductor **308**, the MOS device **300** is able to tolerate a slight misalignment of the conductive plug **322**. This feature will be explained below.

[**0024**] **FIG. 3B** illustrates a cross-section of a MOS device **326** that is the same as the MOS device **300** shown in **FIG. 3A**, except that two conductive plugs **328** are misaligned. The degree of etching of the cap layer **312** by the via etch depends on the preferential nature of the etchant and the particular material or materials in the cap layer **312**. For example, the conductive plug **328** on the left is in contact with the salicide source/drain contact **318**, the insulating sidewall spacer **314**, and the top surface of the insulating cap layer **312** that is at the top of the gate stack. Electrical contact is, as intended, only made to the salicide source/drain contact **318**, since the insulating cap layer **312** insulates the metal gate conductor **308** from being exposed. Thus, a slight misalignment of the conductive plug **328** can be tolerated.

[**0025**] **FIG. 4A** illustrates a cross section of a MOS device **400** constructed on a semiconductor substrate **402**, in accordance with the second embodiment of the present invention. STIs **404** define an active area, on which the MOS device **400** can be formed. A gate dielectric layer **406** is covered by a laterally-recessed metal gate conductor **408** that forms an air void with sidewall spacers **414**. As a design choice, the air void can be filled with a dielectric material, forming side liners **410**, which substantially align with the sidewalls of a cap layer **412**. This laterally-recessed metal gate structure further comprising the spacer formation step to fill the air void and form the spacer layer simultaneously. A low doped drain **411** is formed in a region that extends it to proximity beneath the edge of the metal gate conductor **408**. The cap layer **412**, typically oxide, is deposited on top of the metal gate conductor **408**. The gate stack, composed of the metal gate conductor **408**, the side liners **410** (or air voids) and the cap layer **412**, is covered on their sidewalls by sidewall spacers **414**. Plus-doped source/drain regions **416** are formed on the substrate **402**. A salicide source/drain contact **418** is formed atop the source/drain regions **412**. An inter-level dielectric layer **420** is deposited. A contact via is etched into the inter-level dielectric layer **420**, down to the salicide source/drain contact **418**, and filled with a conductive material, forming a conducive plug **422**. A metal layer is deposited and pattern-etched to form a metal interconnect **424** on the inter-level dielectric layer **420**. Electrical connection is made from the metal interconnect **424**, through the conductive plug **422**, to the salicide source/drain contact **418**. In order to avoid repetition, the choices of design, such as the materials and dimensions of the component structures, are not described in detail here, since they are similar to those introduced by **FIGS. 3A and 3B**.

[**0026**] By using a metal gate conductor **408**, this embodiment avoids the dilemma of choosing between a salicide layer on the poly-silicon gate conductor and a self-aligned contact on the source/drain regions in the conventional art. Furthermore, the cap layer **412** allows the MOS device **400** to tolerate a slight misalignment of the conductive plug **422**, as it will be discussed below.

[**0027**] **FIG. 4B** illustrates a cross section of a MOS device **426** that is the same as the MOS device **400** shown in **FIG. 4A**, except that two conductive plugs **428** are misaligned. The degree of etching of the cap by the via etch depends on the preferential nature of the etchant and the particular material or materials in the cap. In this case, the conductive plug **428** on the left is in contact with the salicide source/drain contact **418**, the insulating sidewall spacer **414**, and the top surface of the cap layer **412** that is at the top of the gate stack. The conductive plug **428** and the salicide source/drain contact **418**, together, are referred to as the self-aligned contact structure. Electrical contact is, as intended, only made to the salicide source/drain contact **418**, since the insulating cap layer **412** and spacers **414** insulate the metal gate conductor **408** from being exposed. In addition, the side liners **410** (see **FIG. 4A**) also increase the isolation margin between the recessed metal gate conductor **408** and the conductive plug **428** that is etched in close proximity. This further adds to the safety margin provided by the sidewall spacer **414**.

[**0028**] **FIG. 5** presents a process flow **500** illustrating the process steps that will produce a MOS device with a combination of a metal gate conductor, and the self-aligned contact structure, in accordance with the first embodiment of the present invention. With reference to both **FIGS. 3A and 5**, in step **502**, the active regions, or the complex areas between the shallow trench isolation (STI) regions **304**, are defined for N-channel or P-channel MOS devices. In step **504**, the channels, or the areas in the substrate **302** immediately beneath the gate dielectric **306**, are doped appropriately. In step **506**, the gate dielectric layer **306** is deposited. In step **508**, the metal gate conductor **308** is deposited. In step **510**, the cap layer **312** is deposited on the metal gate conductor **308**. In step **512**, a gate layer, which is composed of the metal gate conductor **308** and the cap layer **312**, is patterned. In step **514**, the low doped drain **310** is doped. In step **516**, the sidewall spacers **314** are formed. In step **518**, the salicide source/drain contact **318** is doped. In step **520**, a contact etch stop layer, not shown, is deposited. In step **522**, the inter-level dielectric layer **320** is deposited. In step **524**, the inter-level dielectric layer **320** and the cap layer **312** are etched through, down to the metal gate conductor **308**, forming a gate contact opening (not shown). In step **526**, openings for the self-aligned contact structure are patterned